SBC-1 CARD VERSION 8606

Version 8606 is the pre-production prototype of the SBC-1, and if it proves satisfactory on test, will go into production in August 1986. If modifications are required they will be implemented as version 8607.

Setting Up:

Connect U2 EPROM type option Links P2, P3, P4, P5, (Circuit Diagram Sheet 3) according to the type of ROM (usually EPROM) chip in use; see later in this document for full details.

Connect U3 RAM option Links P6, P7 (Circuit Diagram Sheet 3) according to the type of RAM chip in use, see later for full details.

Address Selection Links P13, P14, P15 (Circuit Diagram Sheet 2): Usually EPROM will be at address at address 0000H ("H" = hexadecimal notation throughout what follows), and RAM at 8000H so connect P13 (EPROM) pins 1 and 2, and P14 (RAM) pins 1 and 2. P15 can always have pins 2 and 3 connected, unless one or other (or both) of the EPROM or RAM chips in use is 32K.

I/O Chip Selection Links P12 (Circuit Diagram Sheet 2): Pins 1 and 2 should be connected and pins 3 and 4; this makes the lower of the two 8255's (U6 on Circuit Diagram Sheet 5) IO0(L), and the upper one (U1 on Circuit Diagram Sheet 6) IO1(L).

I/O Chip Software Recommendation: If you can,use the mnemonic significance of the lines IO0 and IO1 - ie IO0 for Output, IO1 for Input.

Use of SBC-1 as I/O Board:

Using the board as an I/O board of the Interak Development System requires the following settings:

Disable CPU	connect P17 pins 2 and 3 (Diagram 3)
Buffer direction:	connect P16 pins 2 and 3 (Diagram 6)
Enable Address Decoding:	connect P8 pins 2 and 3 (Diagram 2)
Disable Buffer from EPROM access	connect P2[illegible] pins 2 and 3 (Diagram 2)
Disable Buffer from RAM access	connect P20 pins 2 and 3 (Diagram 2)
Enable Buffer for IO1 access	connect P22 pins 1 and 2 (Diagram 2)
Enable Buffer for IO0 access	connect P23 pins 1 and 2 (Diagram 2)
Buffer Control Enable Mode	connect P24 pins 2 and 3 (Diagram 2)

The board now operates as a simple I/O board of the Interak. In this application the following components can be omitted: U4 (Z80A-CPU), U2 (EPROM), U3 (RAM), U10 (74HC04), and U11 (74LS14).

The DIL switch S1 should be set to select a convenient group of 8 (or 4 if only one I/O chip is selected via the P22, P23 links) I/O ports which will not clash with existing requirements of the Interak System. (Several of these boards can be plugged into the same system, provided that this requirement is met, and each board is set to a different group of I/O Ports.)

Testing Before Use as Single Board Computer:

For testing the board as a single board computer (with 16K or lesser on-board memories), you should disable the RAM of the Interak for addresses 4000H to BFFFH, ie disable the 4K pages 4, 5, 6, 7, 8, 9, A, B. Then set the SBC-1's EPROM to address 4000H by connecting P13 pins 2 and 3 (Diagram Sheet 2), and enable the data buffer for on-board EPROM and RAM access by connecting both P20 and P21 pins 1 and 2, leaving everything else as above.

The Interak Monitor can now read the SBC-1's EPROM at 4000H, possibly copy parts of it to system RAM address beginning at 0100H in order actually to run the program, and check that the program uses RAM at 8000H, using the monitor to inspect it.

If memory chips larger than 32K are employed then it will become increasingly difficult to make a big enough "hole" in the Interak System memory map for testing of this kind. There are ways of proceeding, but if you are sufficiently experienced to understand the complicated description which would ensue you will be experienced enough to devise such procedures for yourself.

Software recommendation: Let the finished program start in the on-board EPROM at location 0100H; this makes it much easier to develop programs initially in the the Interak CP/M environment. (As the on-board Z80 fetches its first instruction from location 0000H this should contain a jump to the start of the program, ie "C30001" which is a jump to 0100H according to our recommendation.) A further benefit in starting at 0100H is that the various Z80A-CPU "restart" vector areas (in the space below 0100H) are left clear for use, should they be required, eg with interrupts.

Use as a Free-Standing Single Board Computer:

Enable CPU	connect P17 pins 1 and 2 (Diagram 3)
Buffer direction:	connect P16 pins 1 and 2 (Diagram 6)
Disable Address Decoding:	connect P8 pins 1 and 2 (Diagram 2)
Disable Buffer from EPROM access	connect P20 pins 1 and 2 (Diagram 2)
Disable Buffer from RAM access	connect P21 pins 1 and 2 (Diagram 2)
Disable Buffer from IO1 access	connect P22 pins 1 and 2 (Diagram 2)
Disable Buffer from IO0 access	connect P23 pins 1 and 2 (Diagram 2)
Buffer Control Disable Mode	connect P24 pins 1 and 2 (Diagram 2)

The board now operates as a free-standing computer. In this configuration the following components can be omitted: S1 (DIL Switch), U5 (74LS688), U8 (74LS645), U9 (74LS20).

Ganging of Several SBC-1's in a Free Standing System:

* * * WARNING! CHECK ALL THIS BEFORE GENERAL RELEASE! * * *

One of the set of SBC-1's must be designated as the "master". This is the one which is to have the Z80A-CPU. The master has the following sets of connections (assuming that it is to carry the EPROM, RAM, and 2 of the I/O chips of this total small system):

Enable CPU	connect P17 pins 1 and 2 (Diagram 3)
Buffer direction:	connect P16 pins 1 and 2 (Diagram 6)
Enable Address Decoding:	connect P8 pins 2 and 3 (Diagram 2)
Disable Buffer from EPROM access	connect P20 pins 1 and 2 (Diagram 2)
Disable Buffer from RAM access	connect P21 pins 1 and 2 (Diagram 2)
Disable Buffer for IO1 access	connect P22 pins 1 and 2 (Diagram 2)
Disable Buffer for IO0 access	connect P23 pins 1 and 2 (Diagram 2)
Buffer Control Disable Mode	connect P24 pins 1 and 2 (Diagram 2)

No components should be omitted. The DIL switch S1 should be set to select a convenient group of 8 (or 4 if just one 8255 is used) I/O ports.

All the other SBC-1's should be considered to be "slaves". They are wired up in the same way as under the heading "Use as I/O Board" earlier in this document, ie:

Disable CPU	connect P17 pins 2 and 3 (Diagram 3)
Buffer direction:	connect P16 pins 2 and 3 (Diagram 6)
Enable Address Decoding:	connect P8 pins 2 and 3 (Diagram 2)
Disable Buffer from EPROM access	connect P20 pins 2 and 3 (Diagram 2)
Disable Buffer from RAM access	connect P21 pins 2 and 3 (Diagram 2)
Enable Buffer for IO1 access	connect P22 pins 1 and 2 (Diagram 2)
Enable Buffer for IO0 access	connect P23 pins 1 and 2 (Diagram 2)
Buffer Control Enable Mode	connect P24 pins 2 and 3 (Diagram 2)

Each "slave" now operates as a simple I/O board of the "master". In the slave application the following components can be omitted: U4 (Z80A-CPU), U2 (EPROM), U3 (RAM), U10 (74HC04) and U11 (74LS14). The DIL switch S1 on each slave should be set to a different group of I/O ports from each of the other SBC-1's.

If the master has EPROM and RAM each occupying no more than 16K, then a similar quantity can be added on one or other of the slave boards, so that a total of 4 assorted EPROM and RAM memory chips can be achieved. With several SBC-1's in use and a user who has a thorough understanding of the buffering and address decoding arrangements the mixture of RAM and EPROM can be varied, but the standard arrangement of EPROM located in the range 0000H to 7FFFH, and RAM in the range 8000H to FFFFH is straightforward enough to organise with 2 EPROM chips and 2 RAM chips in total, provided no chip is larger than 16K. (Nowadays it is often cheapest to use one large chip for memory instead of several smaller ones, so you must take each case on its merits.)

The maximum number of SBC-1 cards which can be used in the same free standing system is limited by the driving abilities of the Z80A-CPU address lines compared with the total burden of the other cards. The

impedance of the lines connecting the cards together has a bearing too, and is not easy to allow for; but as a rule of thumb 4 or 5 SBC-1 cards closely connected should give no cause for concern of this nature, and will give the very impressive total of 240 individual I/O lines.

Care has been taken in the design to use only those "74LS" series logic devices which are also available in the "74HC" and/or "74HCT" series. These latter types have greatly decreased input current requirements and should be considered if large numbers of SBC-1 cards are connected together in this way, or if the total current consumption of the system is to be minimised.

Similarly the memory chips (EPROM and RAM) can be CMOS for power saving (often RAM is in CMOS anyway), the 8255s can be replaced by 82C55, and the Z80A-CPU by a CMOS Z80.

In short, this design allows for the replacement of every chip by a CMOS equivalent if low power operation is important. (For even lower power with CMOS Z80s the clock rate of the CPU can be lowered from its present 4.0 MHz to 2.0 MHz or even less, provided your program can tolerate the reduced speed of operation, and you can find a crystal of an acceptably small physical size.) If a lower frequency crystal is substituted for Y1, it would be a good idea to increase the value of R3, to reduce the drive to the crystal: as a rough guide to the appropriate value of R3, increase its value until the circuit stops oscillating and then choose a value a quarter or a fifth of this critical value.

The low power CPUs often have a "sleep" mode which enables them to operate with still further reduced power. Sleep mode is entered at a particular clock cycle after a "halt" instruction is executed, and the CPU is only "awoken" by a reset or an interrupt, so if you want to use this mode you will have to ensure that interrupts are provided, and you may have to modify the clock circuit (perhaps with an extra chip, eg the Toshiba T6497 clock generator, on the patch area).

Power Requirements of SBC-1 (Fully Populated):

With standard power chips, 5 volts, typically 300 mA. The current depends somewhat on the number of SIL Resistor packs fitted, and the state of the I/O lines.

With low power (CMOS) chips throughout, estimate ?? 75mA ?? (* * * Check before release * * *).

Commentary on the Design, Choice of Chips etc:

U5 A 74LS688 has been chosen in place of other devices, such as the DM 8131 (etc) comparator. This is not for any technical reason, merely commercial prudence - the 74LS688 is available from several manufacturers and now is cheaper and far easier to obtain.

Another benefit is that a pin-compatible high speed CMOS version, 74HC688, is available.

SIL10 This is normally not fitted. (Its purpose is to pull up TTL logic '1' voltages from about 3V to +5V, in case a 74HC688 is used for U5.)

SIL9, S1 These allows the user to select which group of 8 I/O ports are to be decoded within the development system's I/O space. As U5 in this application is being used only as a 5-bit comparator the lowest 3 comparator inputs are strapped together so that they always match, regardless of the setting of the lowest 3 switches of S1.

U7 This is a type 74LS139. One half is used for (coarse!) decoding of the memory space into "EPROM" and "RAM" areas; the other half separates the chosen 8 I/O ports into two groups of 4; one group for each of the two 8255's, enabled via the chip selects IO0(L) and IO1(L).

Consider the upper, memory, decoder first (Circuit Diagram Sheet 2). This is enabled by the NMREQ signal so that an output will become active (low) for any memory access. As NMREQ goes low during a refresh cycle (NRFSH signal is then also low, but is not used here) then the address decoder U7a will be enabled then as well. This unwanted access enables the data bus buffer U8 (74LS645), but no problem of bus contention occurs because the Z80A-CPU (either the one on the SBC-1 or the one in the Interak system, whichever is in use at the time) deliberately witholds the NRDS signal when it is performing a refresh, so the buffer is left in the "write" direction.

P13, P14, P15:

The 3 pin assemblies P13, P14, P15 are best considered as a group as they act together on U7a (74LS139).

P15 can be linked 1-2 or 2-3. The first position is called "32K" and the second "16K". In the first ("32K") position both inputs A and B of U7 are connected together to address bus line AB15. In operation AB15 of course can be "0" or "1". When it is "0", ie for addresses in the range 0000H-7FFFH, output Y0(L) is active, and if P13 pins 1 and 2 are linked (the "normal" connection) then the EPROM select line goes active (low) so selecting the EPROM socket on the SBC-1 board.

When AB15 is "1", ie for addresses in the range 8000H-FFFFH, output Y3(L) is active, and if P14 pins 2-3 are linked (the "normal" connection) the RAM socket on the SBC-1 board will be selected for addresses in this range.

Note that the precise connections on P13 and P14 have no effect on the decoding in the circumstances so far discussed. No matter what size chips (ie 2K - 32K) are plugged into the EPROM and RAM sockets, they will appear in the memory map at the addresses mentioned above, namely:

```
EPROM  0000H-7FFFH
RAM    8000H-FFFFH
```

32K ROMs and EPROMs do exist eg type 27256, and we believe Hitachi make a 32K RAM (type 65256A, a "pseudo static" 28 pin dynamic RAM). 32K true static RAMs are expected (Hitachi 62256, Toshiba 55257), and can be used if you wish but typical applications of the SBC-1 will be well satisfied by inexpensive chips such as the 2764 (8K EPROM) or 27128 (16K EPROM) and the 6264 (8K RAM). Note that the present RAM socket on the SBC-1 card has not yet been tested with the larger sizes of RAM (this is one of the tests to be carried out on the prototype version 8606).

But back to P15. If pins 2-3 are linked (this is the position we have called "16K"), AB14 is brought into the decoding. There are now 4 possible outputs Y0(L), Y1(L), Y2(L), Y3(L) and the pin assemblies P13 and P14 are brought more fully into play:

```
For EPROM in the range 0000H-3FFFH link P13 pins 1 and 2
For EPROM in the range 4000H-7FFFH link P13 pins 2 and 3
For RAM   in the range 8000H-BFFFH link P14 pins 1 and 2
For RAM   in the range C000H-FFFFH link P14 pins 2 and 3
```

As the ranges above are 16K in extent, memory chips of smaller size will simply repeat throughout the addresses given. Memory chips larger than 16K will only partially appear (but of course if you are using such larger sized memory chips, you would not generally then use a 16K decoding scheme).

As the SBC-1 in its "free standing" application ultimately must have EPROM starting at 0000H (to provide the necessary program for the on-board Z80A-CPU, which of course fetches its first instruction from that location) the second option above would not normally be taken. However it could be useful during development if EPROM could be moved out of its correct location so that it could be read into the development system during the fixing of say some hardware fault. Similarly the RAM can be moved about during testing. For example in a CP/M system which is 48K in extent there is (assuming nothing else is there of course) 16K vacant space at C000H-FFFFH and the RAM can fit conveniently there for testing in the event of trouble during development. CP/M version 2.2 or earlier is very amenable to this kind of work, since a large enough CP/M 2.2 system (say 60K or so) is capable of limited operation with no memory of its own whatever in the 32K range 4000H to BFFFH.

The options so far described are taken by the use of 2 station push fit "JLinks", but if instead flying connections are made eg wire-wrapped, further variations are possible. For example EPROM and RAM can be interchanged in the memory map for fault finding purposes. Another specific example of flexibility in address decoding and selection is when several SBC-1 cards are ganged together to make a "several board single board system" (!). On the master card you could have 16K of EPROM from

address 0000H-3FFFH by linking P13 pins 1 and 2, (with other appropriate links on P14, P15, P20, P21); on one slave you could have a further 16K of EPROM by linking P13 pins 2 and 3, (and the rest appropriately); and on another slave you could have yet more EPROM by linking P14 pin 1 with a flying lead to P13 pin 2, with RAM at the very top of memory (C000H-FFFFH) by linking P14 pins 2 and 3.

Such an EPROM intensive system would be rare, but so would this example offering almost 200 input output lines. It is quoted not so much as a practical suggestion but as a stimulus to help the user recognise the opportunities the SBC-1 presents.

If more EPROM is required at the expense of RAM, note that certain types of EPROMs can also successfully be operated in the socket originally designated for RAM.

Note on Maximum CPU Clock Frequency:

The maximum clock frequency for the Z80 series of microprocessors is mainly decided by the access times of the memories. There are no buffer delays on a single SBC-1, so if all the memory is located on a single SBC-1 (or the master if several SBC-1's are used), then it is very likely that a faster version of the Z80-CPU could be used. The most critical timing for a Z80-CPU operating with no "wait" states (the normal arrangement, although you can add wait states circuitry yourself if you wish) is the "M1 cycle" also called "Op-code Fetch". Data sheets for the faster Z80-CPUs were not to hand when this was being written so the following table must be taken only as a guide.

Chip Type	Max Crystal Frequency	Max Memory Access Time
Z80	2.5 MHz	450 ns
Z80A	4.0 MHz	265 ns
Z80B	6.0 MHz	159 ns (estimate)
Z80H	8.0 MHz	115 ns (estimate)

For the majority of applications examined at the time of writing the Z80A-CPU has been found to be the optimum choice. Typically most if not all of the program code will be located in the EPROM so this is the most critical component in this invstigation. At present it is easy and inexpensive to obtain 8K and upwards EPROMs with 250 ns access times, so they represent the ideal choice.

Remember that the accesses to memory on an SBC-1 card which is not configured as a "master" will be subject to delays through the buffers in the whole system. If it is just for test purposes it will probably be all right to ignore these (because typical memories are much faster than their quoted "worst case" access times), but obviously a rigorous design should be undertaken for something which must be manufactured to guaranteed standards.

If you are not following our recommendations, and get into access time difficulties as a result, you can consider the following ways to overcome them:

Use faster memory chips.
Reduce the Clock frequency.
Add external "wait" state circuitry to op-code fetches and/or to all other memory accesses.

(Note on minimum clock frequency): The usual NMOS Z80A-CPU is partially dynamic inside and will not work correctly if the clock is below a specified minimum frequency; CMOS types on the other hand are usually entirely static and will operate right down to d.c.)

"Halt" Indicator Light(s)

One of the Z80A-CPU outputs is called the "Halt" output, which indicates that the CPU has just executed the HALT instruction. Once this has been executed program flow can only resume or restart if either an interrupt or a reset signal is received by the Z80A-CPU.

The SBC-1 design allows for an on-board Red LED to be illuminated when the Z80A-CPU has executed the HALT instruction. An on-board Green LED is driven with an opposite signal so that it is "on" whenever the Red LED is "off" and vice versa.

The use of these lights depends on the circumstances and the programmer's wishes, but an example application (offered merely to stimulate ideas of your own) would be to force the system to be self-checking and to execute the HALT instruction as soon as it has lost control should a self-check fail. For example a process might require the counting of reqular pulses derived from a shaft which should never stop rotating. If a pulse is not received within a certain time the program can conclude something is seriously wrong, make everything safe, and finally execute a HALT instruction to flag the operator's attention via the Red LED. (During normal operation the Green LED would be on, giving some reassurance that the system was OK.)

It might be more suitable in a given application to have the LEDs located off the SBC-1 board. A pin assembly P19 is provided which can connect to remote LEDs via a suitable mating connector if required. The 74HC04 device used for driving the LEDs is only capable of driving one pair of LED's so a choice must be made between the "on board" or "remote" LEDs. P18 is used for this purpose. Connect P18 pins 1 and 2 for "on board" LEDs, pins 2 and 3 for "remote". The current through each LED is typically -*- mA and can be varied by changing the values of R1 and R2 (note that the 74HC04 specification permits an absolute maximum of 25 mA per output, so keep well below this if you can).

A novel type of LED indicator which can be obtained is one which has both Red and Green elements, ie two LEDs, in the same moulding, with common cathodes and separate anodes. The board has been laid out to allow this "bicolour" option, locally or remotely. The bicolour LED should be connected so that its Red element anode and cathode are exactly as they would be if a single Red LED were used. The third wire (the Green element

anode) will then naturally take up the correct position for connection - ie in the hole provided for the purpose on the circuit board for the local LEDs, or pin 3 of P19 for the remote LEDs.

\- - - - - - - -

(See next page for the selections to be made for the various memory chips which can be used on this board.)

LINKS FOR MEMORY CHIPS

EPROM Socket U2

The socket provided on the SBC-1 for U2 is intended for a variety of EPROM types. A 28 pin socket is provided for use with both 24 pin and 28 pin ICs (when using a 24 pin IC then it should be positioned in the lower part of the socket, ie clear of pins 1,2,27,28 of the socket.)

The customisation of the socket to suit the particular type of IC to be used is carried out by means of push fit jumper links (JLinks) on pin assemblies P2, P3, P4. As the SBC-1 is intended to be a high volume cost-effective design for production use, the design only allows for the modern low-priced EPROMs. The following table gives the relevant information.

Favoured EPROM types for maximum storage capacities in brackets: 2764 (8K), 27128 (16K), 27256 (32K).

EPROM Type		P2 Links U2 Pin 23	P3 Links U2 Pin 26	P4 Links U2 Pin 27	Pin Function 23 26 27
2508	1K	1-2	1-2	X	Vpp; Vcc; NC
(2708)	1K	(This obsolescent device is not supported)			
2716	2K	1-2	1-2	X	Vpp; Vcc; NC
2516	2K	1-2	1-2	X	Vpp; Vcc; NC
2716	2K	1-2	1-2	X	Vpp; Vcc; NC
(TMS2716)	2K	(This obsolescent device is not supported)			
2532	4K(=2K)	(Obsolescent device; see below for limited use)			
2732	4K	2-3	1-2	X	All; Vcc; NC
(2564)	8K	(Obsolescent device; see below for limited use)			
2764	8K	2-3	X	1-2	All; NC; PGM(L)
27128	16K	2-3	2-3	1-2	All; A13; PGM(L)
27256	32K	2-3	2-3	2-3	All, A13; A14
27512	64K(=32K)	2-3	2-3	2-3	All; A13; A14

´X´ means "don´t care", ie the setting here is immaterial. ´NC´ means the EPROM requires no connection to this pin.

Note that it is possible to plug without damage a 2532 into a socket set up for the 2716 device; it will then appear as a 2K EPROM, if the 2K program has been placed in the first half of the device.

Similarly it is possible to plug a 2564 into the U2 socket by setting the following links: P2 pins 2-3, P3 pins 1-2, and P4 pins 2-3 (take care that you get P3 correct because pin 26 on the 2564 is internally connected to the +5V supply pin). The 2564 will then appear as a 4K EPROM but the program must be placed in its first and third quarters (because of the unusual All and Al2 signal connections to this type of EPROM). This is so complicated and tedious we simply recommend that the 2564 device not be used.

A 27512 (64K EPROM can be used in a socket set up for a 27256 (32K EPROM); the 27512 then appears as a 32K device if the program it contains has been placed in the last half of the device. To use the whole 64K in this type of EPROM no other memory chips whatever can be fitted in the same system,

changes must be made to the address decoding arrangements, and pin 1 of the EPROM U2 must be isolated from its present +5V connection and patched to address line A15; a hole is provided near U2 pin 1 for this (unlikely) purpose.

Note that no arrangements whatever have been made in this design for the use of RAM in the EPROM socket U2. This is because in the normal application of a simple Z80 computer system the first locations accessed at power on must be in non-volatile memory such as EPROM, not usually RAM. Non-volatile RAMs do now exist, but still they have little use in this design because there is no opportunity to write to them on-board; unless there is a program already present in the U2 socket at power-on the CPU cannot gain sensible control for writing to RAMs, non volatile or otherwise.

RAM Socket U3

The socket provided on the SBC-1 for U3 is intended for several different RAM types. A 28 pin socket is provided for use with both 24 pin and 28 pin ICs (when using a 24 pin IC then it should be positioned in the lower part of the socket, ie clear of pins 1,2,27,28 of the socket.)

The customisation of the socket to suit the particular type of RAM to be used is carried out by means of push fit jumper links (JLinks) on pin assemblies P6 and P7. The following table gives details.

We recommend the following RAM types for maximum storage capacities given in brackets, but a full list is given in the table below: 6116/6117/5517 (2K), 5564/5565/6264 (8K), 55257/62256 (32K).

RAM Type		P5 Links U3 Pin 1	P6 Links U3 Pin 23	P7 Links U3 Pin 26	Pin Function 1 23 26
4118	1K	X	1-2	1-2	NC; R/W; Vcc
4801	1K	X	1-2	1-2	NC; R/W; Vcc
2016	2K	X	1-2	1-2	NC; R/W; Vcc
48Z02	2K	X	1-2	1-2	NC; R/W; Vcc
(5516)	(2K)	(This unusual variant not supported; no OE(L) pin)			
5517	2K	X	1-2	1-2	NC; R/W; Vcc
(5518)	(2K)	(This unusual variant not supported; no OE(L) pin)			
6116	2K	X	1-2	1-2	NC; R/W; Vcc
6117	2K	X	1-2	1-2	NC; R/W; Vcc
5564	8K	X	2-3	1-2	NC; A11; CS2(H)
5565	8K	X	2-3	1-2	NC; A11; CS2(H)
6264	8K	X	2-3	1-2	NC; A11; CS2(H)
55257	32K	1-2	2-3	2-3	A14; A11; A13
62256	32K	1-2	2-3	2-3	A14; A11; A13
65256	32K	(Requirements unknown at present)			

'X' means "don't care"; 'NC' means the RAM requires no connection to this pin.

Using EPROMs in the RAM socket

Because of the close similarity between the families of 28 pin RAMs and EPROMs it is also possible to use certain EPROM types in the "RAM" socket U3. Each case should be investigated by the user before proceeding, but our own preliminary examinations suggest that there should be no difficulty in using the following types of EPROM in the manner discussed below:

EPROM Type		P5 Links U3 Pin 1	P6 Links U3 Pin 23	P7 Links U3 Pin 26	Pin Function 1 23 26
2764	8K	2-3	~~1-2~~ 2-3	X	Vpp; A11; NC
27128	16K	2-3	~~1-2~~ 2-3	2-3	Vpp; A11; A13
27256	32K(as 16K)	2-3	~~1-2~~ 2-3	2-3	Vpp; A11; A13
27512	64K(as 16K)	2-3	~~1-2~~ 2-3	2-3	A15; A11; A13

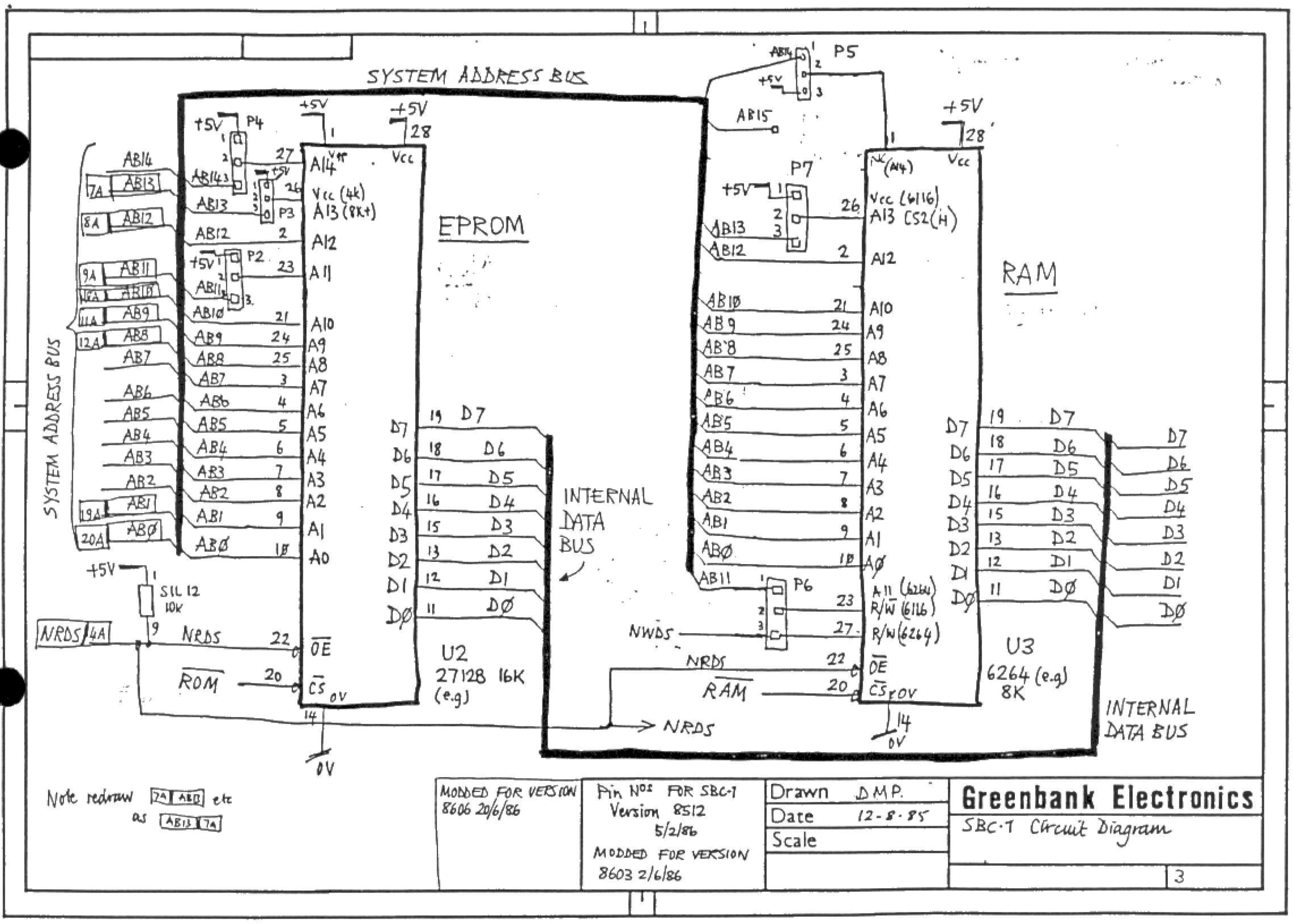
"X" = "don't care"; 'NC' means the EPROM requires no connection to this pin.

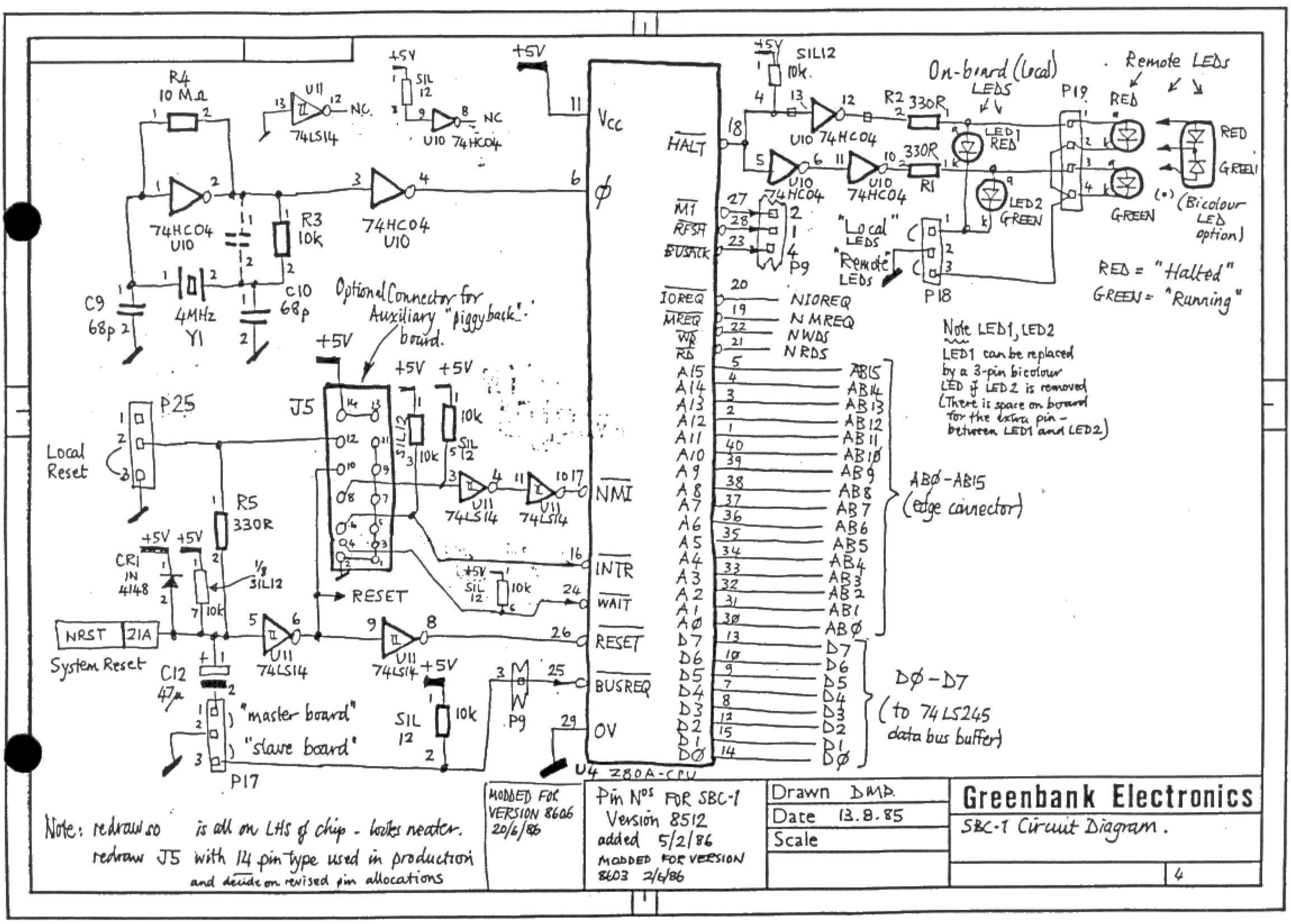
The reader might be alarmed if he studies the pinouts in detail for the 2764 and 27128 because these two have a signal "PGM(L)" (the programming control) of the EPROM at pin 27 and in our design the U3 socket NWDS (the "write" strobe) is connected to this pin, thus PGM(L) will be pulsed in the event of an inadvertent "write" to the U3 socket. However no unwanted programming takes place here because to program an EPROM requires that it first be placed in "programming" mode. This can only be done by raising the voltage on pin 1 (for the types under discussion) to a specified higher voltage than +5V, therefore it is impossible to enter programming mode for these EPROMs in this design.

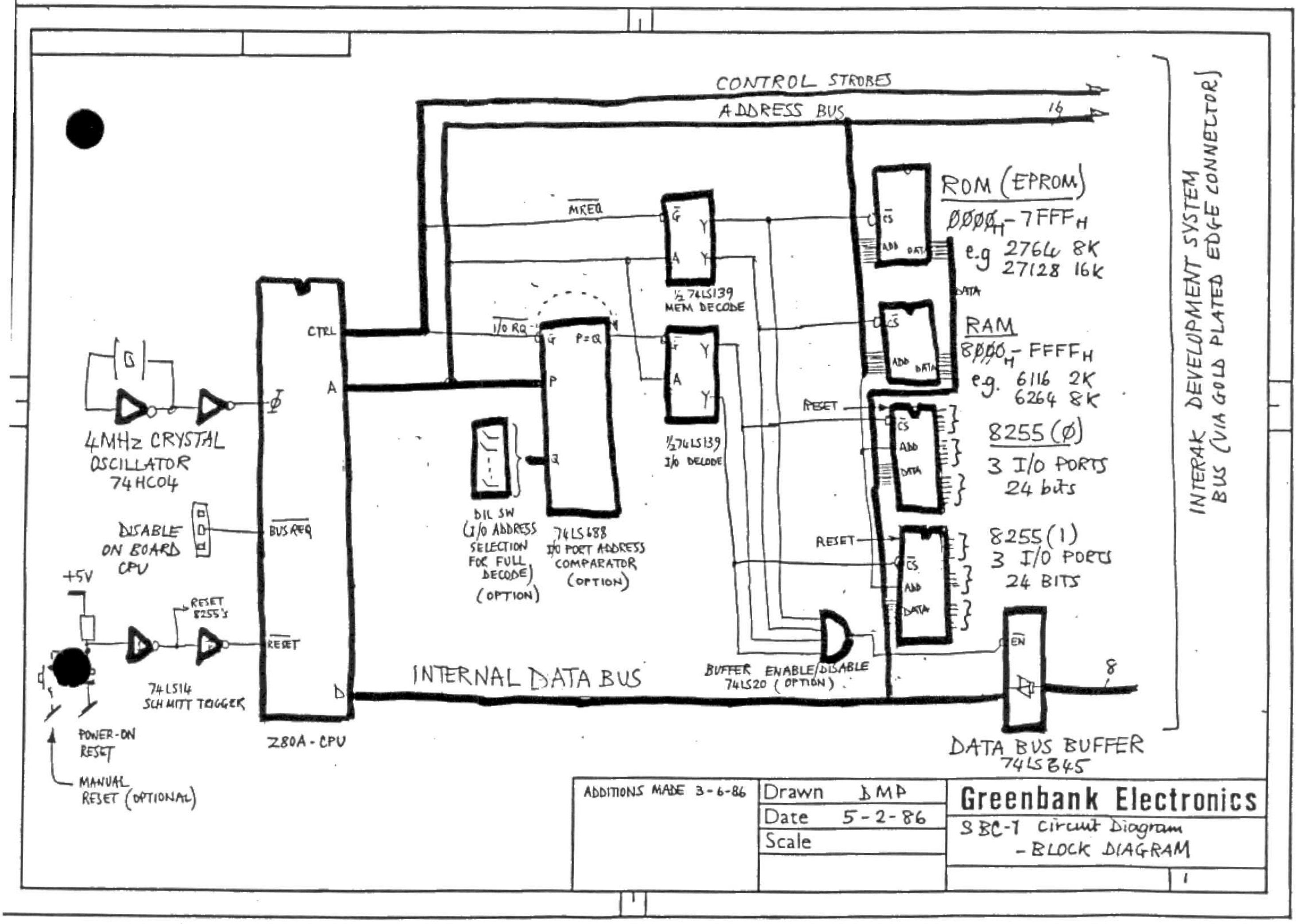
The last two entries in the table are for 27256 and 27512 type EPROMs, nominally 32K and 64K respectively. Both these types can be plugged into the U3 socket without damage (if it is set up as for a 27128) but they then will appear only as 16K types (because the EPROM and RAM pinouts utilise different pins for the higher order address lines, A14 and A15 - these could have been accomodated in this design at the expense of more jumper links and consequent complexity, but this option was not taken because this would be satisfying the needs of the minority at the expense of the majority). If you want to use a 27256 or 27512 EPROM in the U3 RAM socket, limited to 16K use as described, then you should program the 16K into the last 16K in the EPROM in each case.

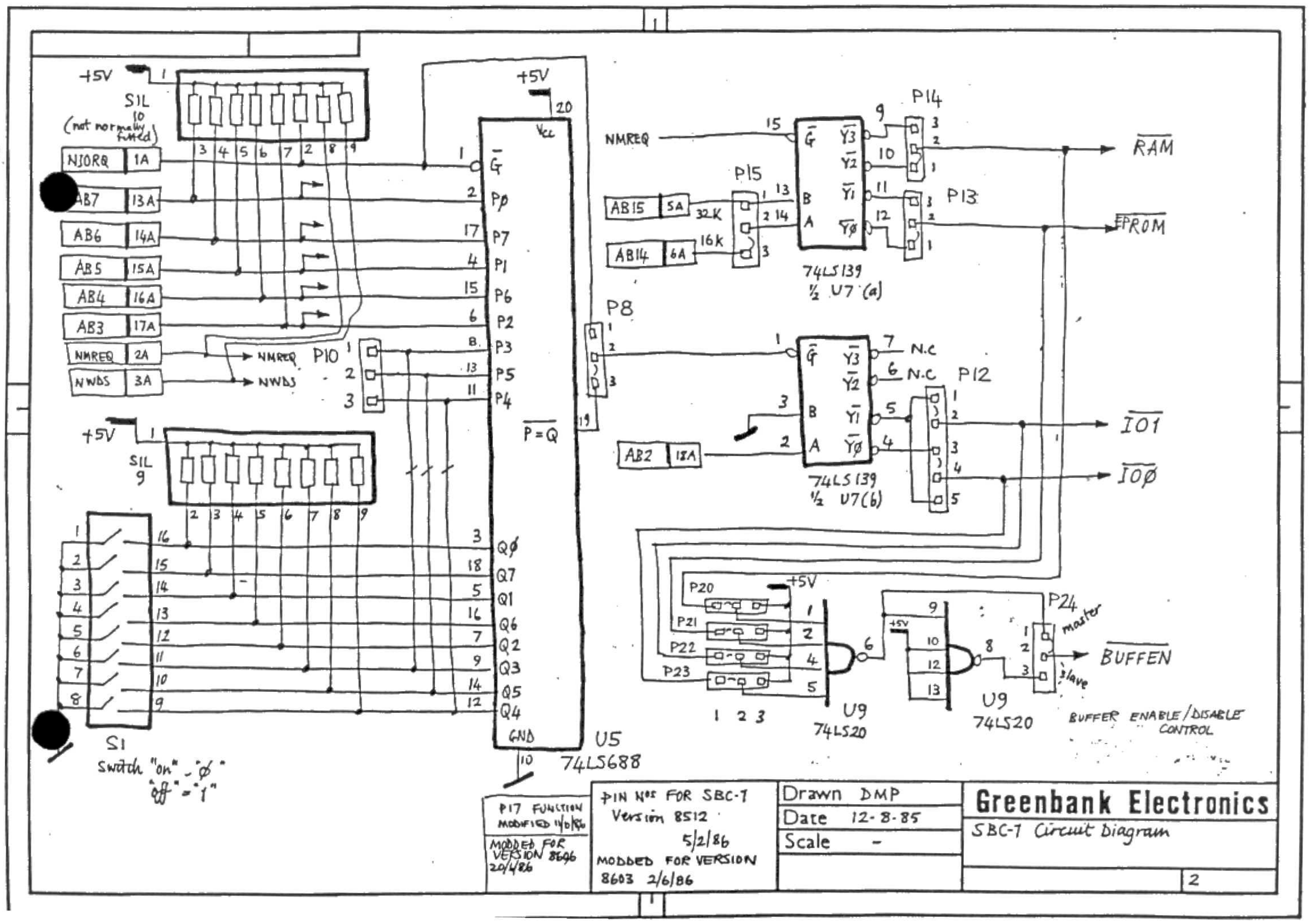
D M Parkins 19th June 1986
Telephone 051-645 3391

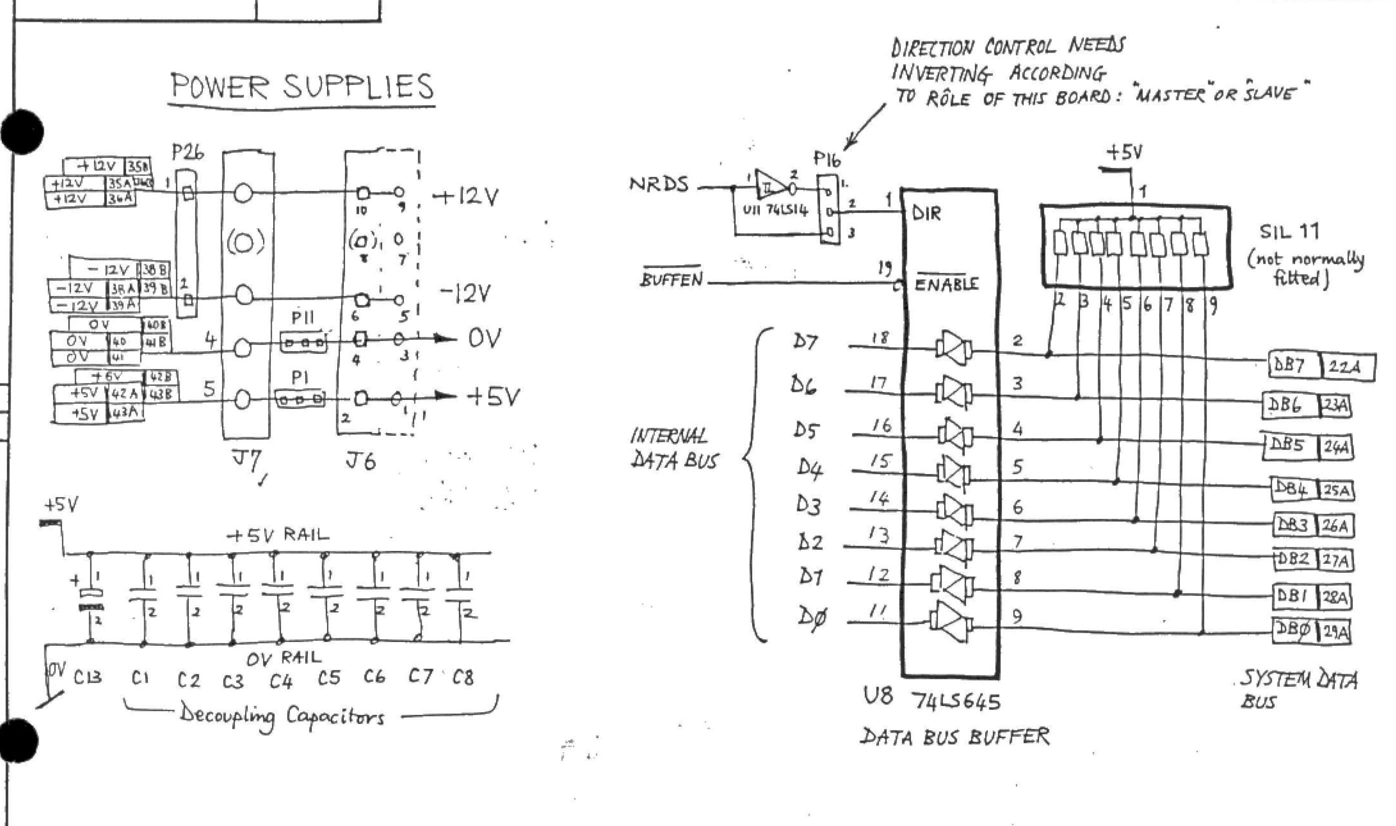
Greenbank Electronics


SYSTEM ADDRESS BUS
EPROM
RAM
INTERNAL DATA BUS
U2 27128 16K (e.g)
U3 6264 (e.g) 8K
NRDS
ROM
RAM
NWDS
SIL 12 10k
P2 P3 P4 P5 P6 P7
Note redraw 7A AB12 etc as AB13 7A
MODDED FOR VERSION 8606 20/6/86
Pin N^os FOR SBC-1 Version 8512 5/2/86
MODDED FOR VERSION 8603 2/6/86
Drawn DMP.
Date 12-8-85
Scale
Greenbank Electronics
SBC-1 Circuit Diagram
3

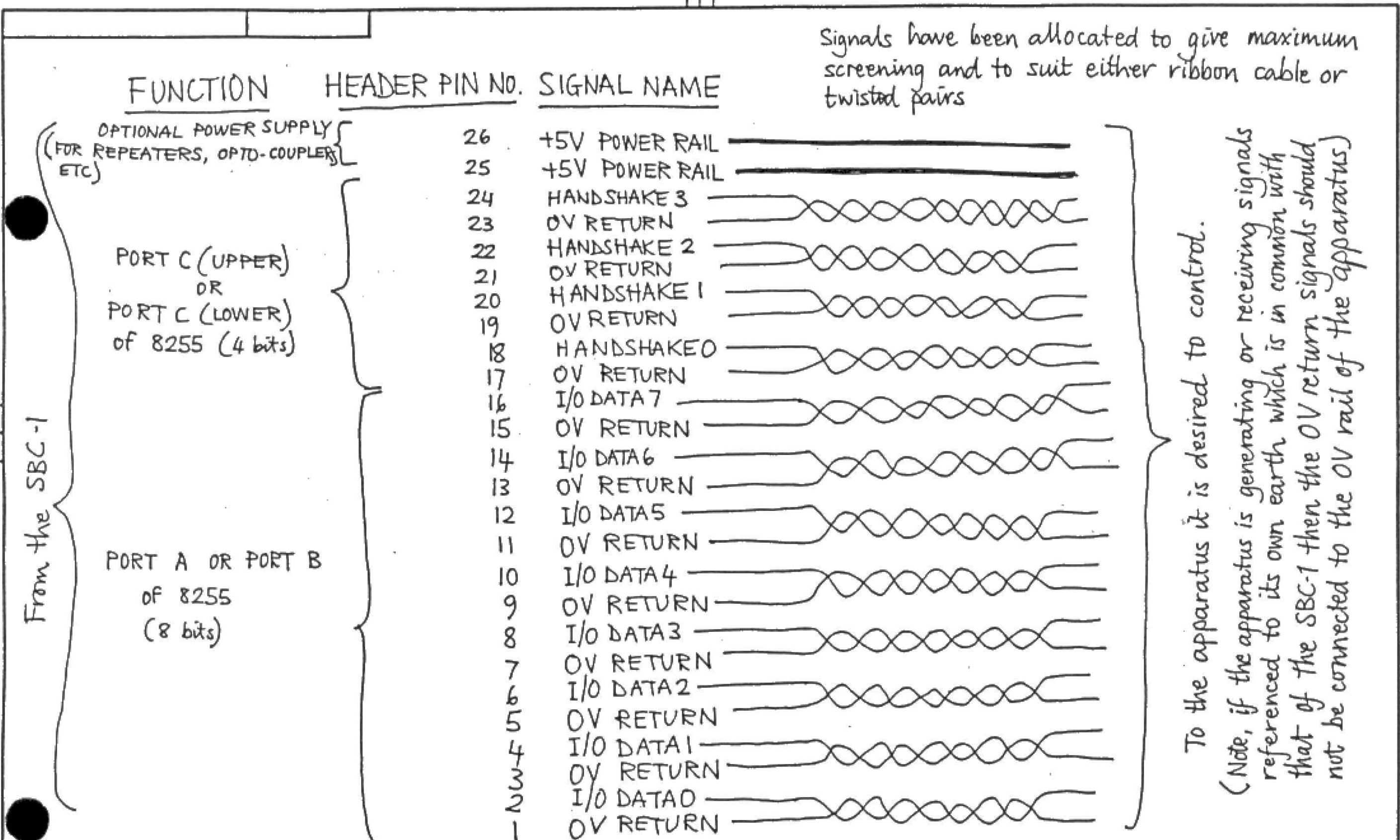

R4 10 MΩ
74HC04 U10
R3 10k
C9 68p
4MHz Y1
C10 68p
Optional Connector for Auxiliary "piggyback" board.
J5
P25
Local Reset
R5 330R
CR1 1N 4148
C12 47µ
NRST 21A
System Reset
"master board"
"slave board"
P17
RESET
74LS14
U11
NMI
INTR
WAIT
BUSREQ
HALT
U4 Z80A-CPU
On-board (Local) LEDS
Remote LEDs
RED
GREEN
(Bicolour LED option)
RED = "Halted"
GREEN = "Running"
"Local" LEDS
"Remote" LEDS
P18 P19 P9
NIOREQ
NMREQ
NWDS
NRDS
ABØ-AB15 (edge connector)
DØ-D7 (to 74LS245 data bus buffer)
Note LED1, LED2
LED1 can be replaced by a 3-pin bicolour LED if LED2 is removed (There is space on board for the extra pin - between LED1 and LED2)
Note: redraw so is all on LHS of chip - looks neater. redraw J5 with 14 pin type used in production and decide on revised pin allocations
MODDED FOR VERSION 8606 20/6/86
Pin N^os FOR SBC-1 Version 8512 added 5/2/86
MODDED FOR VERSION 8603 2/6/86
Drawn DMP.
Date 13.8.85
Scale
Greenbank Electronics
SBC-1 Circuit Diagram.
4


CONTROL STROBES
ADDRESS BUS
16
ROM (EPROM)
ØØØØH - 7FFFH
e.g 2764 8K
27128 16K
RAM
8ØØØH - FFFFH
e.g. 6116 2K
6264 8K
8255 (Ø)
3 I/O PORTS
24 bits
8255 (1)
3 I/O PORTS
24 BITS
INTERAK DEVELOPMENT SYSTEM
BUS (VIA GOLD PLATED EDGE CONNECTOR)
MREQ
½ 74LS139
MEM DECODE
½ 74LS139
I/O DECODE
I/O RQ
P=Q
74LS688
I/O PORT ADDRESS
COMPARATOR
(OPTION)
DIL SW
(I/O ADDRESS
SELECTION
FOR FULL
DECODE)
(OPTION)
CTRL
A
D
Z80A - CPU
4MHz CRYSTAL
OSCILLATOR
74HC04
DISABLE
ON BOARD
CPU
BUSREQ
+5V
RESET
8255's
RESET
74LS14
SCHMITT TRIGGER
POWER-ON
RESET
MANUAL
RESET (OPTIONAL)
INTERNAL DATA BUS
BUFFER ENABLE/DISABLE
74LS20 (OPTION)
EN
8
DATA BUS BUFFER
74LS245
ADDITIONS MADE 3-6-86
Drawn DMP
Date 5-2-86
Scale
Greenbank Electronics
SBC-1 Circuit Diagram
- BLOCK DIAGRAM
1


+5V
SIL
10
(not normally fitted)
NIORQ 1A
AB7 13A
AB6 14A
AB5 15A
AB4 16A
AB3 17A
NMREQ 2A
NWDS 3A
NMREQ
NWDS
P10
+5V
SIL
9
S1
switch "on" - "Ø"
"off" - "1"
+5V
20
Vcc
G
PØ
P7
P1
P6
P2
P3
P5
P4
P=Q
QØ
Q7
Q1
Q6
Q2
Q3
Q5
Q4
GND
U5
74LS688
P8
NMREQ
AB15 5A
AB14 6A
32K
16K
P15
74LS139
½ U7 (a)
P14
P13
RAM
EPROM
N.C
N.C
P12
AB2 18A
74LS139
½ U7 (b)
IO1
IOØ
P20
P21
P22
P23
+5V
U9
74LS20
U9
74LS20
P24
master
slave
BUFFEN
BUFFER ENABLE/DISABLE
CONTROL
P17 FUNCTION
MODIFIED 1/6/86
MODDED FOR
VERSION 8606
20/6/86
PIN NOS FOR SBC-1
Version 8512
5/2/86
MODDED FOR VERSION
8603 2/6/86
Drawn DMP
Date 12-8-85
Scale -
Greenbank Electronics
SBC-1 Circuit Diagram
2

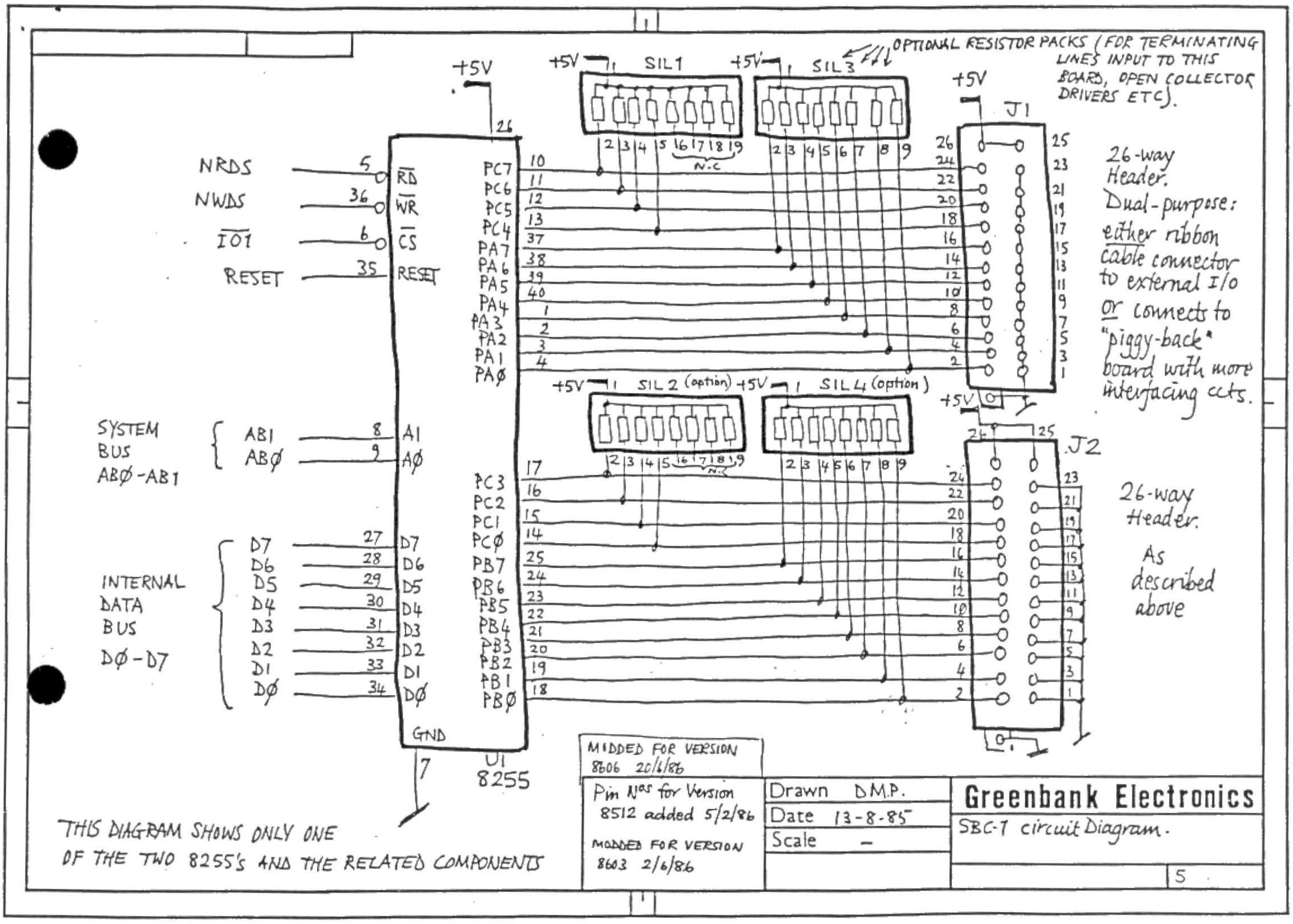


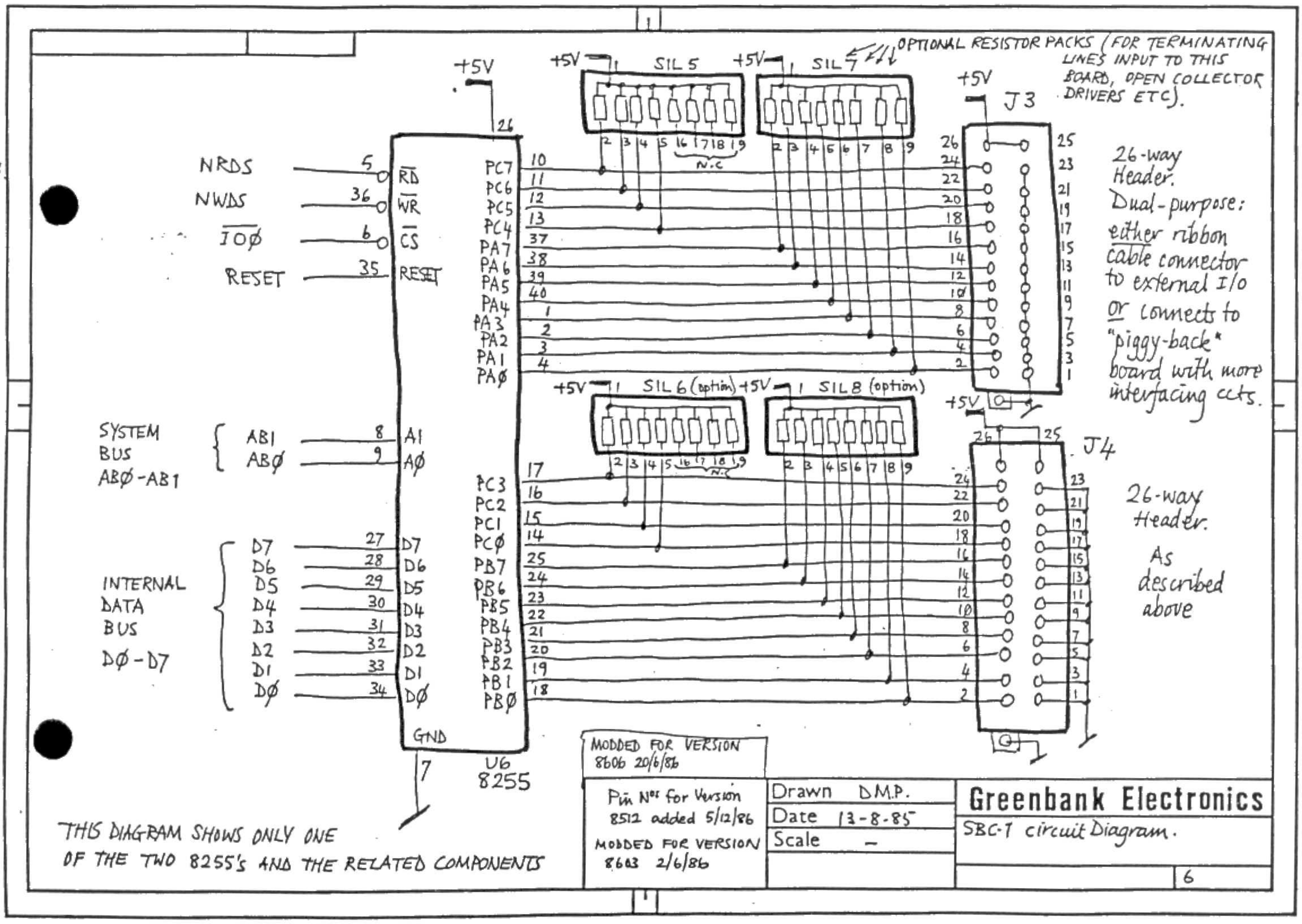
MODDED FOR VERSION 8606 20/6/86	Pin nos for version 8512 added 5/12/86 MODDED FOR VERSION 8606 2/6/86	Drawn DMP Date 12-8-85 Scale -	**Greenbank Electronics** SBC-1 Circuit Diagram 7

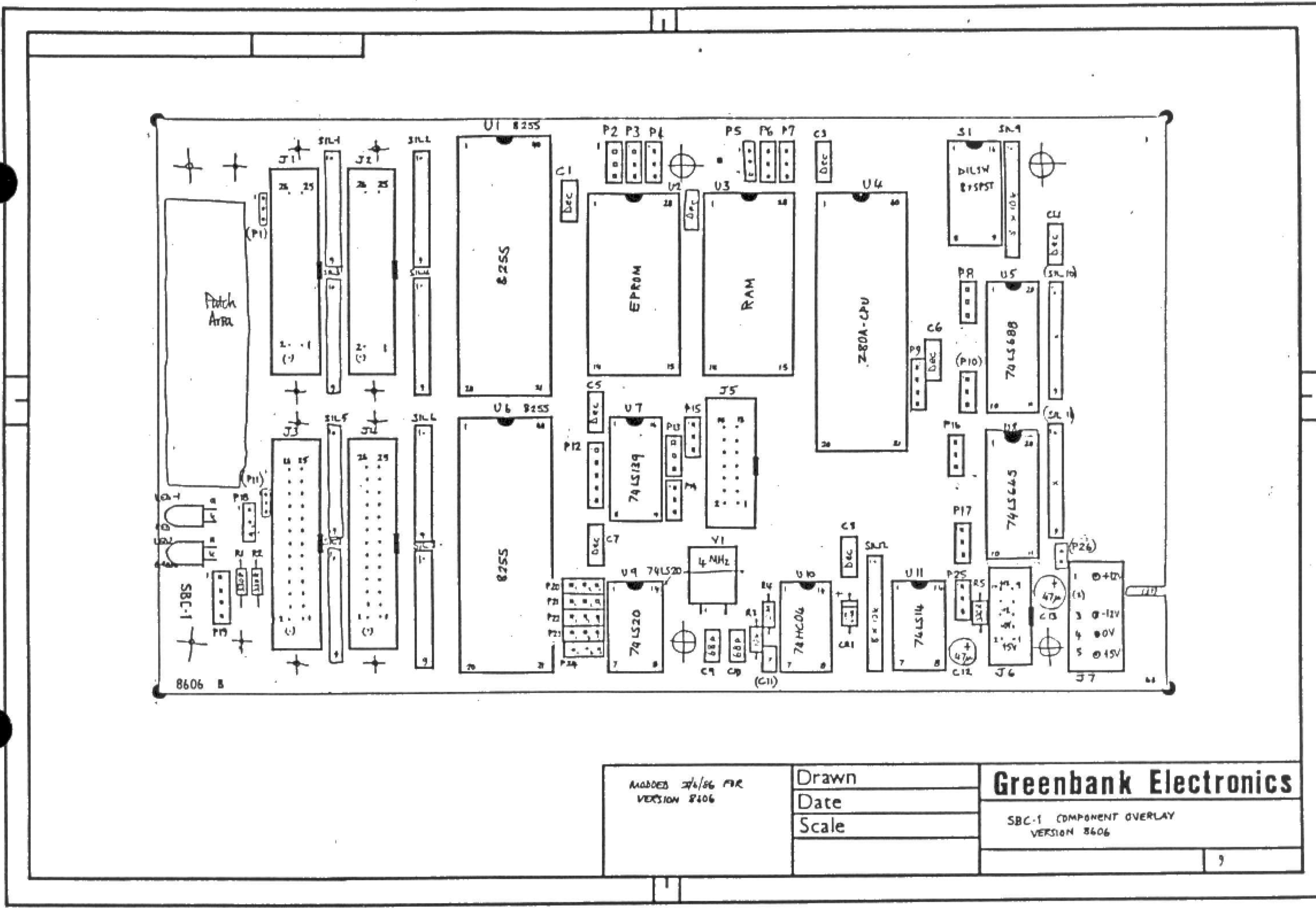


THE ARRANGEMENT SHOWN IS FOR JUST ONE OF THE FOUR CONNECTORS. THE OTHER 3 ARE THE SAME.

ALL VERSIONS.	Drawn D.M.P. Date 7-2-86 Scale -	**Greenbank Electronics** SBC-1 I/O ALLOCATIONS FOR SIGNAL CONNECTORS 8


+5V
NRDS
NWDS
IO1
RESET
RD
WR
CS
PC7
PC6
PC5
PC4
PA7
PA6
PA5
PA4
PA3
PA2
PA1
PAØ
SIL1
SIL3
OPTIONAL RESISTOR PACKS (FOR TERMINATING LINES INPUT TO THIS BOARD, OPEN COLLECTOR DRIVERS ETC).
N.C
J1
26-way Header. Dual-purpose: either ribbon cable connector to external I/O or connects to "piggy-back" board with more interfacing cts.
SIL2 (option)
SIL4 (option)
J2
SYSTEM BUS ABØ-AB1
AB1
ABØ
A1
AØ
PC3
PC2
PC1
PCØ
PB7
PB6
PB5
PB4
PB3
PB2
PB1
PBØ
26-way Header. As described above
INTERNAL DATA BUS DØ-D7
D7
D6
D5
D4
D3
D2
D1
DØ
GND
U1
8255
THIS DIAGRAM SHOWS ONLY ONE OF THE TWO 8255's AND THE RELATED COMPONENTS
MODDED FOR VERSION 8606 20/6/86
Pin N[os] for Version 8512 added 5/2/86
MODDED FOR VERSION 8603 2/6/86
Drawn D.M.P.
Date 13-8-85
Scale –
Greenbank Electronics
SBC-1 circuit Diagram.
5


+5V
NRDS
NWDS
IOØ
RESET
RD
WR
CS
PC7
PC6
PC5
PC4
PA7
PA6
PA5
PA4
PA3
PA2
PA1
PAØ
SIL5
SIL7
OPTIONAL RESISTOR PACKS (FOR TERMINATING LINES INPUT TO THIS BOARD, OPEN COLLECTOR DRIVERS ETC).
N.C
J3
26-way Header. Dual-purpose: either ribbon cable connector to external I/O or connects to "piggy-back" board with more interfacing cts.
SIL6 (option)
SIL8 (option)
J4
SYSTEM BUS ABØ-AB1
AB1
ABØ
A1
AØ
PC3
PC2
PC1
PCØ
PB7
PB6
PB5
PB4
PB3
PB2
PB1
PBØ
26-way Header. As described above
INTERNAL DATA BUS DØ-D7
D7
D6
D5
D4
D3
D2
D1
DØ
GND
U6
8255
THIS DIAGRAM SHOWS ONLY ONE OF THE TWO 8255's AND THE RELATED COMPONENTS
MODDED FOR VERSION 8606 20/6/86
Pin N[os] for Version 8512 added 5/12/86
MODDED FOR VERSION 8603 2/6/86
Drawn D.M.P.
Date 13-8-85
Scale –
Greenbank Electronics
SBC-1 circuit Diagram.
6



NOTE: THERE ARE SOME CHANGES TO THIS LIST FOR VERSION 8606

COMPONENT PRICE LIST FOR SBC-1 CARD "Master" Config List Ref: SBC-1M/PO
(Prices exclude VAT) February 1986

Prices each, ex.VAT

Resistors 0.25W (0.4")						
CR25330R	3	R1,2,5		0.02	0.06	
CR2510K	1	R3		0.02	0.02	
CR2510M	1	R4		0.02	0.02	
SIL Resistors (Use 9-pin Sockets)						
not used	10	SIL1-8,10,11		-	-	
SIL8-10K	2	SIL9,12		0.26	0.52	
	7(17)		Resistor Pack RSBC1M		0.62	0.62
Capacitors						
("Al" = Low Leakage Miniature Aluminium Electrolytic; "Cer" = Ceramic; "Dec" = 47n-100n Decoupling grade polyester, or Ceramic)						
not used	1	C11		-	-	
CER68P	2	C9,10		0.05	0.10	
47n-100n Dec	8	C1-8		0.09	0.72	
47u Al	2	C12,13		0.10	0.20	
	12(13)		Capacitor Pack CSBC1M		1.02	1.02
Diodes						
1N4148	1	CR1		0.04	0.04	
RLED5 0.2" Red	1	LED1		0.14	0.14	
GLED5 0.2" Grn	1	LED2		0.12	0.12	
	3		Diode Pack DSBC1M		0.30	0.30
Quartz Crystal						
4.0M	1	Y1		1.75	1.75	
	1		Quartz Crystal YSBC1M		1.75	1.75
Integrated Circuits (Use Sockets)						
not inc	1	U1 8255	(40 pin)	-	-	
not inc	1	U2 ROM	(28 pin)	-	-	
not inc	1	U3 RAM	(28 pin)	-	-	
not inc	1	U5 74LS688	(20 pin)	-	-	
not inc	1	U8 74LS645	(20 pin)	-	-	
not inc	1	U9 74LS20	(14 pin)	-	-	
8255A	1	U6	(40 pin)	4.00	4.00	
74HC04	1	U10	(14 pin)	0.36	0.36	
74LS14	1	U11	(14 pin)	0.49	0.49	
Z80A-CPU	1	U4	(40 pin)	3.25	3.25	
74LS139	1	U7	(16 pin)	0.54	0.54	
	5(11)		Integrated Circuit Pack ICSBC1M		8.64	8.64
DIL Switch						
not inc	1	S1 DILSW8	(16 pin)	-	-	-
DIL & SIL Sockets						
9SCON	12	SIL1-12		0.06	0.72	
DIL14	3	U9,10,11		0.10	0.30	
DIL16	2	S1; U7		0.10	0.20	
DIL20	2	U5,8		0.22	0.44	
DIL28	2	U2,3		0.28	0.56	
DIL40	3	U1,4,6		0.30	0.90	
	24		DIL & SIL Socket Pack SKSBC1M		3.12	3.12

List continues on next page

SBC-1 COMPONENT PRICE LIST ("MASTER") continued List Ref: SBC-1M/PO

0.1" Pitch Pin Assemblies					
not used	1	P8 PINASY3	-	-	
not used	1	P7,22 PINASY5	-	-	
PINASY3	18	P1-6,10-16,18-21,23	0.11	1.98	
PINASY4	1	P17	0.14	0.14	
PINASY5	1	P9	0.15	0.15	
	22	Pin Assembly Pack PNSBC1M		2.27	2.27
Sundry					
IDCPSLP26	4	J1-4	1.34	5.36	
IDCPSLP10	1	J6 (was 5-way on v 8512)	0.74	0.74	
IDCPSLP14	1	J5 (was 10-way on v 8512)	0.88	0.88	
PL156S5	1	J7	0.40	0.40	
JLinks	20	JL1-20	0.20	4.00	
	22	Sundry Pack SYSBC1M		11.38	11.38

Total cost of kit of all parts listed so far: PSBC1M 29.10

OPTIONS (i.e. Items not included in standard kit of parts)

Prices each, ex. VAT

SBC-1 p.c.b, sold separately as "BSBC1"	BSBC1	17.50
Manual, sold separately as "MSBC1" (Zero Rated for VAT)	MSBC1	3.00 OZ
Power Connector with 4 wires 1m length	LD4P156	1.20
Ribbon Cable per metre: 14 way IDCR14 0.78; 26 way	IDCR26	1.50
IDC cable socket (female): 14 way IDCF14 1.44; 26 way	IDCF26	2.14
Circuit board socket (female): 10 way IDPFS10 2.38; 14 way IDCPFS14 2.82; 26 way	IDCPFS26	3.86
Studded M3 13mm spacer kit with fixings (Set of 6)	O1SB1	1.00

Add 50p handling charge to each transaction, and 15% VAT.

SIL8-1K0, SIL8-10K, SIL8-100K, (each)		0.26
450ns 2K x 8 EPROM	2716	3.90
450ns 4K x 8 EPROM	2732	4.25
250ns 8K x 8 EPROM	2764	2.75
250ns 16K x 8 EPROM	27128	5.50
250ns 32K x 8 EPROM	27256	15.00
150ns 2K x 8 RAM	6116	2.75
150ns 8K x 8 RAM	6264	5.20
3 x 8-bit I/O Ports	8255A	4.00
Dual 4-i/p NAND	74LS20	0.36
Octal Tranceiver	74LS645	1.32
8-bit Comparator	74LS688	3.50
8 x SPST DIL Switch	DILSW8	1.50
3-pin 0.1" Pin assembly	PINASY3	0.11
5-pin 0.1" Pin assembly	PINASY5	0.15